IN THE CLAIMS

1. (currently amended) A method for producing yield enhancement data for integrated circuits on a substrate, the method comprising ~~the~~ steps of:

comparing a database of physical defects on the substrate to a database of design information for the integrated circuits, and

associating the physical defects on the substrate with classes of design information by location on the substrate of both the physical defects and elements of the design information to produce the yield enhancement data.

2. (currently amended) The method of claim 1, wherein the database of physical defects comprises a physical defect wafer map.

3. (currently amended) The method of claim 1, wherein the physical defects on the substrate are optically observable physical defects.

4. (original) The method of claim 1, wherein the design information includes structures formed in the integrated circuits.

5. (original) The method of claim 1, wherein the classes of design information comprises classes of physical structures.

6. (currently amended) The method of claim 1, further comprising ~~the~~ a step of creating the database of physical defects by inspections of the substrate, where the inspections are conducted at multiple times during fabrication of the integrated circuits.

7. (currently amended) The method of claim 1, further comprising ~~the~~ a step of creating the database of design information from design files for the integrated circuits.

8. (currently amended) The method of claim 1, further comprising ~~the~~ a step of revising the design information based at least in part on the yield enhancement data.

9. (currently amended) A method for producing yield enhancement data from integrated circuits on a substrate, the method comprising ~~the~~ steps of:

creating a database of design information for the integrated circuits, which design information is used as a template for fabricating the integrated circuits, where the design information includes structure location information for physical structures used to form the integrated circuits,

binning the physical structures in the design information in the database of design information as belonging to at least one of a number of different classes of physical structures,

creating a database of physical defects on the substrate during inspections of the substrate that are conducted during processing of the integrated circuits, where the physical defects listed in the database of physical defects are associated with physical defect location information,

comparing the database of design information with the database of physical defects to create associations between the design information and the physical defects based on matching the structure location information with the physical defect location information, and

reporting the physical defects based on the classes of the design information with which they are associated as a result of the comparison, to produce the yield enhancement data.

10. (currently amended) The method of claim 9, wherein the database of physical defects comprises a physical defect wafer map.

11. (currently amended) The method of claim 9, wherein the physical defects on the substrate are optically observable physical defects.

12. (canceled)
13. (canceled)
14. (canceled)

15. (currently amended) The method of claim 9, further comprising ~~the~~ a step of revising the design information based at least in part on the yield enhancement data.

16. (currently amended) A computerized system for analyzing physical defects, the computerized system comprising:

means for receiving design information for integrated circuits, where the integrated circuits are fabricated on a substrate based on the design information, where the design information includes structure location information for physical structures used to form the integrated circuits,

means for binning the physical structures in the design information in ~~the~~ a database of design information as belonging to at least one of a number of different classes of physical structures,

means for receiving physical defect information for integrated circuits, where the physical defect information contains locations of physical defects on the substrate,

means for comparing the design information with the physical defect information based on matching the structure location information with the locations of physical defects on the substrate, and

means for associating the physical defects with the classes of the design information based on physical proximity on the substrate to produce yield enhancement data.

17. (currently amended) The computerized system of claim 16, wherein the physical defect information comprises a physical defect wafer map.

18. (original) The computerized system of claim 16, further comprising means for revising the design information based at least in part on the yield enhancement data.

19. (canceled)
20. (canceled)